

CLAIMS

- 1 1. An RF power LDMOS transistor comprising:
 - 2 - multiple pairs of parallel gate fingers, the gate fingers of each gate finger pair being
 - 3 located on opposite sides of an associated p+ sinker, and metal clamps being provided
 - 4 to short-circuit the p+ sinkers and n+ source regions on opposite sides of the p+
 - 5 sinkers,
 - 6 - wherein each gate finger of a gate finger pair is associated with separate metal
 - 7 clamps that short-circuit the n+ source region and the p+ sinker associated with that
 - 8 particular gate finger,
 - 9 - wherein the separate metal clamps associated with each gate finger pair are separated
 - 10 by a slot that extends between the parallel gate fingers,
 - 11 - a metal runner that extends in the slot between the separate metal clamps associated
 - 12 with each gate finger pair from a gate pad, and
 - 13 - wherein both gate fingers of a gate finger pair are connected to the associated metal
 - 14 runner at both their ends and at predetermined positions along their lengths.
- 1 2. The transistor according to claim 1, wherein the metal runners are provided on
- 2 a dielectric layer on top of the p+ sinkers.
- 1 3. The transistor according to claim 1, wherein each metal clamp covers the
- 2 associated gate finger to shield it from a respective drain region.
- 1 4. The transistor according to claim 1, further comprising a well which extends
- 2 from under the gate fingers and encloses said source regions.
- 1 5. The transistor according to claim 4, further comprising source regions
- 2 extending lateral from each side of said well.

1 6. The transistor according to claim 5, wherein the source region comprise a first
2 region and a second region surrounding said first region, wherein the second region is
3 less doped than said first region.

- 1 7. An RF power LDMOS transistor comprising:
 - 2 - a substrate,
 - 3 - a first and second source region spaced apart,
 - 4 - a sinker separating said first and second source region,
 - 5 - a first and second drain region arranged to define in combination with said first and
 - 6 second source region a first and second channel,
 - 7 - a first and second gate finger covering said first and second channel, respectively,
 - 8 - first and second metal clamps which short-circuit the sinker and respective source
 - 9 regions on opposite sides of the sinker,
 - 10 - wherein the first and second metal clamps are separated by a slot that extends
 - 11 between the parallel gate fingers, and
 - 12 - a metal runner that extends in the slot between the separate metal clamps.
- 1 8. The transistor according to claim 7, wherein both gate fingers are connected to
- 2 the associated metal runner at both their ends and at predetermined positions along
- 3 their lengths.
- 1 9. The transistor according to claim 7, wherein the metal runner is provided on a
- 2 dielectric layer on top of the sinker.
- 1 10. The transistor according to claim 7, wherein each metal clamp covers the
- 2 associated gate finger to shield it from a respective drain region.
- 1 11. The transistor according to claim 7, further comprising a well which extends
- 2 from under the gate fingers and encloses said source regions wherein said well defines
- 3 the channel.

1 12. The transistor according to claim 7, wherein each source region comprise a
2 first region and a second region surrounding said first region, wherein the second
3 region is less doped than said first region.